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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,513	01/27/2004	Hidenori Nanki	56937-108	9962

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EXAMINER	
KROPCHECK, MICHAEL C	
ART UNIT	PAPER NUMBER
2186	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/764,513	NANKI ET AL.	
	Examiner	Art Unit	
	MICHAEL C. KROFCHECK	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-5 and 11-13* is/are allowed.

6)☒ Claim(s) *6-10 and 14-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to amendment filed on 7/15/2008.

2. Claims 6-10 and 20 have been amended.

3. New claims 22-26 have been added and examined.

4. The objections and rejections from the prior correspondence that are not restated herein are withdrawn.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

7. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 6, 14-15, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham et al. (US 5237616), Ishimoto et al. (US 6101586), Koizumi (US 5414864), and Guttag et al. (US 4590552).

9. With respect to claim 6, Abraham teaches of an information processing apparatus for accessing memory spaces including a user memory space and a secure memory space (fig. 1; item 105, 109), comprising: a secure bit generating unit for receiving data and determining which of the user memory space and the secure memory space is indicated by address information (column 2, lines 57-67, as data is restricted from accessing a memory in either circumstance, it is abundantly clear to one of ordinary skill in the art that there is something that determines which memory the access is directed to through its address), and

delivering the received data the secure bit into a general purpose register including a secure bit unit, the general purpose register having a function of receiving and holding the data with the secure bit added thereto (fig. 1; column 2, lines 45-48; the Intel 80C186 processor inherently contains general purpose registers used for arithmetic operation and I/O operation. Intel's "80C186EA/80C188EA Microprocessor

User's Manual" provides support for this in sections 2.1, 2.1.3 on pages 2-1, 2-4 to 2-5. The secure bit is that of Guttag);

a built-in memory space for receiving and holding the data with the secure bit from the general purpose register and delivering the data with the secure bit to the general purpose register (fig. 1; item 105, 109; the secure bit is that of Guttag); and

a data output control unit having a function of controlling a data transfer to an external space by using the secure bit (column 2, lines 57-67; the secure bit is that of Guttag);

wherein the data output control unit performs a control operation to determine whether the data transfer to the external space is prohibited or not by a value of the secure bit (column 2, lines 57-67; column 3, lines 10-12; the secure bit is that of Guttag).

Abraham fails to explicitly teach of adding a secure bit to the received data based on determining which of the user memory space and the secure memory space is indicated by the address information associated with the received data.

Guttag teaches of a secure bit generating unit for receiving data and determining which of the user memory space and the secure memory space is indicated by address information associated with the received data (fig. 3; column 6, lines 34-38),

adding a secure bit to the received data based on determining which of the user memory space and the secure memory space is indicated by the address information associated with the received data (fig. 3; column 6, lines 45-53)

a data output control unit having a function of controlling a data transfer to an external space by using the secure bit (fig. 3; column 6, lines 53-56);

wherein the data output control unit performs a control operation to determine whether the data transfer to the external space is prohibited or not by a value of the secure bit (fig. 3; column 6, lines 53-56).

Abraham fails to explicitly teach of the built-in memory space being a RAM. However, Ishimoto teaches of the built-in memory space being a RAM (column 11, lines 46-49).

Abraham fails to explicitly teach of a value of the secure bits being set in the general purpose register. However, Koizumi teaches of a status value being set in the general purpose register (column 2, lines 36-42).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham and Guttag at the time of the invention to tag the data as protected or not in Abraham as taught in Guttag to create more flexibility as to how the data is managed.

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Guttag, and Ishimoto at the time of the invention to use RAM as the unprivileged memory in the combination of Abraham and Guttag as taught in Ishimoto, since RAM is the most commonly available and most versatile type of memory.

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Guttag, Ishimoto, and Koizumi at the time of the invention to indicate the privileged and unprivileged states in the GPR of the combination of Abraham, Guttag, and Ishimoto as taught in Koizumi so the status is directly accessible by the processor.

10. With respect to claim 14, Guttag teaches of wherein the data control unit determines whether the data transfer to the user memory space is prohibited or not irrespective of a mode associated with a CPU (column 2, lines 3-54).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi, and Guttag at the time of the invention to determine the allowability of data transfer independently of the CPU in the combination of Abraham, Ishimoto, Koizumi as taught in Guttag so that the protection of software is extended against numerous external peripheral devices (Guttag, column 1, lines 65-68).

11. With respect to claim 15, Abraham teaches of wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode (column 2, lines 57-61).

12. With respect to claim 22, Guttag teaches of wherein adding the secure bit to the received data includes: adding a first value to the received data based on determining that the user memory space is indicated by the address information associated with the received data (column 6, lines 34-38 and lines 45-49; the bit is not 'set' when the address does not indicate protected memory. This is the equivalent to adding a value of zero), and

adding a second value to the received data based on determining that the secure memory space is indicated by the address information associated with the received data (column 6, lines 34-38 and lines 45-49).

13. Claims 9, 18-19 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham, Guttag, Ishimoto, Koizumi and Banno et al. (5680581).

14. With respect to claim 9, the combination of Abraham, Guttag, Ishimoto, and Koizumi teach of the limitations cited above with respect to claim 6.

Abraham fails to explicitly teach of a direct memory access unit with a secure bit unit having a function of holding a secure bit. However, Banno teaches of a computer system including a direct memory access controller (column 1, lines 11-15; in the combination the DMA controller also stores the secure bit of Guttag since it is a part of the data).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi and Banno at the time of the invention to incorporate the DMA controller of Banno into the combination of Abraham, Ishimoto, Koizumi. Their motivation would have been to allow for data transfer to take place without the processor controlling it, thus creating more available processing time.

15. With respect to claim 18, Guttag teaches of wherein the data control unit determines whether the data transfer to the user memory space is prohibited or not irrespective of a mode associated with a CPU (column 2, lines 3-54).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi, Banno, and Guttag at the time of the invention to determine the allowability of data transfer independently of the CPU in the combination of Abraham, Ishimoto, Koizumi and Banno as taught in Guttag so that the protection of software is extended against numerous external peripheral devices (Guttag, column 1, lines 65-68).

16. With respect to claim 19, Abraham teaches of wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode (column 2, lines 57-61).

17. With respect to claim 25, Guttag teaches of wherein adding the secure bit to the received data includes: adding a first value to the received data based on determining that the user memory space is indicated by the address information associated with the received data (column 6, lines 34-38 and lines 45-49; the bit is not 'set' when the address does not indicate protected memory. This is the equivalent to adding a value of zero), and

adding a second value to the received data based on determining that the secure memory space is indicated by the address information associated with the received data (column 6, lines 34-38 and lines 45-49).

18. Claims 7-8, 10, 16-17, 20-21, 23-24, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham, Guttag, Ishimoto, Koizumi, Banno, and Garney, (5386552).

19. With respect to claim 7, the combination of Abraham, Guttag, Ishimoto, and Koizumi teach of the limitations cited above with respect to claim 6.

Abraham fails to explicitly teach of delivering an instruction with a secure bits into an instruction decoder including a secure bit unit, the instruction decoder having a function of determining which of the user memory space and the secure memory space is associated with the instruction under execution.

However, Banno teaches of delivering an instruction with a secure bits into an instruction decoder with a secure bit unit, the instruction decoder having a function of

determining which of the user memory space and the secure memory space is associated with the instruction under execution (column 3, lines 44-51);

Abraham fails to explicitly teach of an interrupt saved information unit including a secure bit unit, the interrupt saved information unit having a function of adding, upon generation of an interrupt process, the secure bit of the instruction decoder to data saved in a stack area of the built-in RAM space.

However, Garney teaches of a built-in RAM space with a secure bit for receiving and holding the data with a secure bit from the general purpose register and delivering the data with secure information held to the general purpose register (column 1, lines 17-40; in the combination in an interrupt processing or context switch, the GPR from the processor of Abraham are saved in the stack of Garney);

an interrupt saved information unit including a secure bit unit, the interrupt saved information unit having a function of adding, upon generation of an interrupt process, the secure bit of the instruction decoder to data saved in a stack area of the built-in RAM space (column 1, lines 17-40).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Guttag, Ishimoto, Koizumi, and Banno at the time of the invention to identify the memory associated with the requested instruction in the combination of Abraham, Guttag, Ishimoto, and Koizumi as taught in Banno. Their motivation would have been to prevent a third party from gaining knowledge of the internal program (column 1, lines 20-24).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Guttag, Ishimoto, Koizumi, Banno, and Garney at the time of the invention store the processor context upon an interrupt occurrence in the combination as taught in Garney. Their motivation would have been to enable multitasking, thus increasing the efficiency of the processor.

20. With respect to claim 8, the combination of Abraham, Guttag, Ishimoto, Koizumi, Banno, Garney teach of the limitation cited above with respect to claim 7.

Garney also teaches of a stack pointer for defining a part of the built-in RAM space as the stack area (column 1, lines 25-29; it is abundantly clear to one of ordinary skill in the art that a stack comprises stack pointers which define the stack); and

a saved information rewrite control unit for controlling a rewrite operation in the stack area of the built-in RAM space (column 1, lines 25-29; it is abundantly clear to one of ordinary skill in the art that since data is written to and from the stack, there must be something that controls this);

The combination of Abraham, Guttag, Ishimoto, Koizumi, Banno, Garney teaches of wherein the saved information rewrite control unit prohibits the rewrite operation if the instruction of the instruction decoder is associated with the user memory space and intended to rewrite the stack area of the built-in RAM space (since in the combination, writing something that does not originate within the internal memory to an internal memory is inhibited by the protection circuit of Banno, writing state information involving instruction not from the internal memory into an internal RAM stack would not be allowed).

21. With respect to claim 10, the combination of Abraham, Guttag, Ishimoto, Koizumi, Banno, Garney teach of the limitation cited above with respect to claim 7.

Banno teaches of an operating unit including a secure bit unit having a function of reflecting the secure bit of the instruction decoder in an arithmetic operation executed in accordance with the instruction decoded by the instruction decoder (column 1, lines 55-65, column 3, lines 44-56).

22. With respect to claims 16 and 20, Guttag teaches of wherein the data control unit determines whether the data transfer to the user memory space is prohibited or not irrespective of a mode associated with a CPU (column 2, lines 3-54).

It would have been obvious to one of ordinary skill in the art having the teachings of Abraham, Ishimoto, Koizumi, Banno, Garney, and Guttag at the time of the invention to determine the allowability of data transfer independently of the CPU in the combination of Abraham, Ishimoto, Koizumi, Banno, and Garney as taught in Guttag so that the protection of software is extended against numerous external peripheral devices (Guttag, column 1, lines 65-68).

23. With respect to claims 17 and 21, Abraham teaches of wherein the mode associated with the CPU includes a privileged mode or an unprivileged mode (column 2, lines 57-61).

24. With respect to claims 23-24 and 26, Guttag teaches of wherein adding the secure bit to the received data includes: adding a first value to the received data based on determining that the user memory space is indicated by the address information associated with the received data (column 6, lines 34-38 and lines 45-49; the bit is not

'set' when the address does not indicate protected memory. This is the equivalent to adding a value of zero), and

adding a second value to the received data based on determining that the secure memory space is indicated by the address information associated with the received data (column 6, lines 34-38 and lines 45-49).

Allowable Subject Matter

25. Claims 3-5, 11-13 are allowed.

Response to Arguments

26. Applicant's arguments with respect to the independent claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

27. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

28. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

29. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Krofcheck whose telephone number is 571-272-8193. The examiner can normally be reached on Monday - Friday.

30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

31. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/MICHAEL C KROFCHECK/
Examiner, Art Unit 2186

/Matt Kim/
Supervisory Patent Examiner, Art Unit 2186

Michael Krofcheck